EECS 3201 :: Lab 5
Simulation with ModelSim

Administrative Instructions

Demonstration: Labs must be demonstrated during lab periods on the week of November 9-13. You may demonstrate your lab on an earlier week with the permission of the TA, but only during your designated lab period.

The TAs will be extremely busy towards the end of the lab. You are **strongly advised** to prepare as much as possible in advance, work efficiently in the lab, and to demonstrate as early as possible. **Leaving the demonstration to the last minute is at your own risk.**

Group composition: You may work in groups of **at most two**. Working by yourself is OK if there is enough equipment. Groups of three or larger are **not allowed.** There is no need to stay with the same lab partner as in previous labs, but you can if you want to.

To make the best use of your time in the lab, you should write your Verilog code beforehand. You can then use the lab time to debug your code. For this lab, note that you *do not need the DE10-Lite,* everything can be done on the computer.

Scoring: This lab is scored out of 5 marks.

- *Demonstration:* Once done, you will demonstrate your work to the TA. Correctly demonstrating the result is worth 3 marks. If you can't get the design to work, you can still demonstrate, but you will lose marks. *You will get a grade of zero if you don't demonstrate anything by the end of the lab period.*
- *Question:* The TA will ask **each** group member a question, for example to modify the circuit. Correctly answering the question is worth 2 marks.

It is possible for group members to receive different grades, for example, different grades can be received on the question.

Value: This lab is worth 2/10 of your total lab score and 2% of your final grade.

Problem

In this lab you will write testbench modules to test circuits in ModelSim.

Having trouble running ModelSim on your home computer? Historically, students who run Linux on their own laptops had trouble running ModelSim. This was because ModelSim relies on 32-bit libraries which are not installed with 64-bit Linux distributions by default. It is not clear if this has been fixed in the current version of ModelSim. If not, there are various instructions for getting ModelSim to work, for example:

https://mil.ufl.edu/3701/docs/quartus/linux/ModelSim_linux.pdf

You might also ask your favorite LLM for help.

Testbenches

Download modules test1.v and test2.v from eClass. The first file, test1.v, is a combinatorial circuit with three inputs and two outputs; the second file, test2.v, is a sequential circuit with two inputs (one of which is the clock), and a four-bit bus output.

Write testbench modules as follows:

- For test1.v, write a testbench that tests all 8 possible input values, and holds each of these input values for 20 nanoseconds. If (and only if) both outputs are zero, the testbench should write the message “All outputs are zero” to the simulation console. Save the testbench in: test1_tb.v
- For test2.v, generate a clock with a 20 nanosecond period (10 ns on and 10 ns off) and provide it to the circuit. The other input should be 0 for the first 100 ns, 1 for the next 200 ns, and 0 for all time afterward. If (and only if) all outputs are zero, the testbench should write the message “All outputs are zero” to the simulation console. Save the testbench in: test2_tb.v

In the lab:

- Write and compile your testbenches. Check for errors and fix them. (You don’t need the DE10-Lite board for this.)
- Once you are happy with your testbenches, demonstrate them to the TA. The TA may ask to see your Verilog module, and will also ask each group member a question about your design.